

# High Performance Computing Modernization Program (HPCMP) Summer 2011 Puerto Rico Workshop on Intermediate Parallel Programming & Cluster Computing

in conjunction with  
the National Computational Science Institute (NCSI)/  
SC11 Conference



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Jointly hosted at  
Polytechnic U of Puerto Rico  
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(streaming video recordings coming soon)



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# Intermediate Parallel Programming & Cluster Computing Storage Hierarchy Review



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Sunday July 31 – Saturday August 6 2011



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# Since it is a review, lets review

When it comes to Intermediate Parallel Programming,

- What is the Storage Hierarchy?
- What is important relative to parallel programming?



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# What is the Storage Hierarchy?

- Progression from fast, small, expensive storage (registers) to slow, big, cheap storage (disk/network)
  - register ( $\sim 350\text{GB/sec}$ )
  - -> Level 1 cache ( $\sim 250\text{GB/sec}$ ) ( $\sim 70\%$  of register)
  - -> Level n cache (balances effect of Level 1 cache and RAM)
  - -> RAM ( $\sim 10\text{GB/sec}$ ) ( $\sim 3\%$  of register)
  - -> Disk/network ( $\sim 100\text{MB/sec}$ ) ( $\sim .03\%$  of register)
- Parallel architectures -> complicated storage hierarchies
  - Shared memory and thread local
  - Memory local to each computational node
  - GPU Register, Local, Shared, Global, Constant, Texture



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# What is important relative to parallel programming?

- Performance comes from overlapping CPU and IO
- Storage is advancing at slower rates than CPUs  
effective data movement is more and more important
- Problem and algorithm help inform what to do
- Worth doing if can solve problems otherwise unreachable



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# Getting a drink An Analogy

- I live in East Bay about 35 miles from San Francisco
- RAM is walking 50 feet to the refrigerator
- Lev 1 cache is walking 100 feet to the garage
- RAM is driving 1/3 mi to the grocery store
- Disk/Network is driving to San Francisco



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**Thanks for your  
attention!**



**Questions?**