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Relative performance is calculated by assigning a baseline value of 1.0 to one benchmark result, and then dividing the actual benchmark result for the baseline platform into each of the specific benchmark results of each of the other platforms, and assigning them a relative performance number that correlates with the performance improvements reported.

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Notice revision #20101101
1 TRILLION
\((10^{12})\)
1 TRILLION
($10^{12}$)

projected number of connected machines and devices by 2022

Source: Trillion Sensors Summit, October 2013
40% of FORTUNE500 companies in 2000 were out in 2010.

To Compete You Must Compute.
Intel in the Datacenter

CLOUD Platform

BIG DATA Platform

TC/HPC Platform
The Path to Discovery & Innovation

EXPERIMENT
Observation

THEORY
Mathematical Model

TC/HPC
Numerical Simulation

\[
\begin{align*}
\frac{\partial u}{\partial t} &+ \frac{u \partial u}{r} - \frac{v^2 + w^2}{r} = \frac{\partial p}{\partial x} + g \rho \frac{\partial h}{\partial x} \\
\frac{1}{\sin \theta} \frac{\partial^2 u}{\partial \theta^2} &+ \frac{\partial u}{\partial \alpha} = \frac{\partial}{\partial \phi} \left( \frac{u \partial u}{r} + 2 \frac{\partial h}{\partial \phi} \right) \\
\frac{1}{\sin \theta} \frac{\partial^2 v}{\partial \theta^2} &+ \frac{\partial v}{\partial \alpha} = -\frac{1}{r^2} \frac{\partial}{\partial \phi} \left( \frac{u \partial v}{r} - \frac{2}{r^2} \cos \theta \frac{\partial h}{\partial \phi} \right) \\
\frac{1}{\sin \theta} \frac{\partial^2 w}{\partial \theta^2} &+ \frac{\partial w}{\partial \alpha} = \frac{\partial}{\partial \phi} \left( \frac{w \partial w}{r} - \frac{2}{r^2} \cos \theta \frac{\partial h}{\partial \phi} \right)
\end{align*}
\]

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The Path to Discovery & Innovation

TECH COMPUTING / HPC

Numerical Simulation  Big Data Analytics  Visualization
HPC Led Discoveries

Astrophysics | Life-Science | Climate | Manufacturing
---|---|---|---
Energy | Financial | Weather | Security

www.hpcwire.com/2014/01/02/top-supercomputing-discoveries-2013/

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What does it mean? for Science, Industry and Economics

- Better products – faster and cheaper
- Safer transportation (cars, trains, airplanes, boats, ...)
- Better and more robust structures (bridges, buildings, machinery, ...)
- Better materials and reduced material scrapping
- Resource efficient material
- Secure, clean, efficient and sustainable energy
- Reducing fuel consumption and CO₂ emission (fuel efficiency)
- Generate more Oil&Gas reserves
- New energy resources (solar, wind, hydro)
- Improved Weather, severe storm, fire, flooding and earthquake prediction (catastrophe prevention)
- Better Disease control (fewer diseases and lower costs)
- Improved cancer treatment
- Better medicine, well-being, healthcare
- Better Bio-Economy (food&water security, sustainable agriculture)
- Better Cyber Security and electronic fraud control
HPC Opportunities for SMBs

Better Products
More Products
More Features
Faster Time to Market
More Efficient
Cheaper

www.comsol.com
HPC Opportunities for SMB
Multiphysics Simulations

High Performance Computing (HPC)

- Addresses the world’s hardest computational problems
- Performed on high-performance server nodes connected with high-performance fabrics

The Cluster is the System
STRATEGY:
If it computes, it does it best with Intel
HPC IMPERATIVES

- High Performance
  Capabilities & Capacity

- Energy Efficiency
  TCO

- Ease of Use
  Productivity & Sustainability
Two Computing/Competing Universes

More Performance
More Memory
More Bandwidth
More Storage
More Speed
More Resiliency
More ...

Less Power
Less Space
Less Complexity
Less Programming
Less Management
Less Costs
Less ...

MORE

LESS
Integrated Electronics
Transforming the Economics of HPC

Executing to Moore’s Law

Predictable Silicon Track Record – well and alive at Intel. Enabling new devices with higher performance and functionality while controlling power, cost, and size

**Future options are forecasts and subject to change without notice.**
First Conflict-Free Processors

Photo: Sasha Lezhnev
World's First Conflict-Free Microprocessors

What are Conflict Minerals?
Conflict Minerals are metals that come from the Democratic Republic of Congo (DRC), a place where violent militias and rebel groups control trade, exploit workers, and finance violence.

What has Intel done?
Intel, along with partners, created an audit and verification system that supports responsible sourcing of minerals from the DRC and the pursuit of conflict-free supply chains.

1 Intel has manufactured the world’s first commercially available “conflict-free” processors. “Conflict-free” means “DRC conflict-free”, which is defined by the Securities and Exchange Commission rules to mean products that do not contain conflict minerals (tin, tantalum, tungsten and/or gold) that directly or indirectly finance or benefit armed groups in the Democratic Republic of the Congo (DRC) or adjoining countries.

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Driving Innovation and Integration
Enabled by Leading Edge Process Technologies

Integrated Today

Coming Tomorrow**

SYSTEM LEVEL BENEFITS IN COST, POWER, DENSITY, SCALABILITY & PERFORMANCE

**Future options are forecasts and subject to change without notice.
From MILLIWATTS to TERAFLOPS

Smartphones with Intel® Inside

Intel® Xeon® Processors

Intel® Many Integrated Core Architecture

Energy Efficient
The Magic of Integration
Moore's Law at Work & Architecture Innovations

1970s
150 MFLOPS
CRAY-1*

2013
1000000 MFLOPS
Intel® Xeon Phi™

6666x
Intel Technical Computing
The Right Tool for the Job: A Continuum of Computing

Desktop
See a simple result

Tablet

Intel® Xeon® Workstation
More results, faster
Better teamwork
Faster turns

Local Cluster Computation
More simulations
Breakthrough ideas & research

Large Clusters
Change the world
Discover the unknown
Transformational insight

Common underlying architecture
scales investments across technical computing platforms

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**Intel Technical Computing Portfolio**

<table>
<thead>
<tr>
<th>Product</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® based Workstations/Visualization</td>
</tr>
<tr>
<td>Intel® Cluster Ready (ICR)</td>
</tr>
<tr>
<td>Intel® Data Center Manager (DCM)</td>
</tr>
<tr>
<td>Intel® SW Development Tools</td>
</tr>
<tr>
<td>Intel® Big Data Analytics Toolkit</td>
</tr>
<tr>
<td>Intel® Enterprise Edition Lustre (Filesystem)</td>
</tr>
<tr>
<td>Intel® SSDs (NVMe)</td>
</tr>
<tr>
<td>Intel® based Storage</td>
</tr>
<tr>
<td>Intel® True Scale Fabric (IBA)</td>
</tr>
<tr>
<td>Intel® Networking (10/40GbE)</td>
</tr>
<tr>
<td>Intel® Boards &amp; Systems</td>
</tr>
<tr>
<td>Intel® Xeon Phi™ Coprocessor</td>
</tr>
<tr>
<td>Intel® Xeon® Processors</td>
</tr>
</tbody>
</table>

**INTEL TECHNICAL COMPUTING & HPC SOLUTIONS PORTFOLIO**

All components working “better together” for a comprehensive and high-performance end-to-end solution based on Intel technologies.
Intel Technical Computing & HPC Technologies

Compute Processing

Systems & Boards

Network & Fabric

I/O & Storage

Software & Services

*Other names and brands may be claimed as the property of others.
„Big Core“ – „Small Core“

Intel® Xeon® Processor

Simply aggregating more cores generation after generation is not sufficient

Performance per core/thread must increase each generation, be as fast as possible

Power envelopes should stay flat or go down each generation

Balanced platform (Memory, I/O, Compute)

Cores, Threads, Caches, SIMD

Intel® Xeon Phi™ Coprocessor

Optimized for highest compute per watt

Willing to trade performance per core/thread for aggregate performance

Power envelopes should also stay flat or go down every generation

Optimized for highly parallel workloads

Cores, Threads, Caches, SIMD

For illustration only

*Other names and brands may be claimed as the property of others.
Modernize Your Software!
Performance = Parallelism on all Levels

Theoretical acceleration of a highly parallel processor over a Intel® Xeon® parallel processor (<1: Intel® Xeon® faster) – For illustration only

- **NODES** clustering
- **SIMD** vectorization
- **CORES** multi-threading
- **ILP** instruction parallelism
Parallel is Your Path Forward

General Purpose and Fully Programmable Hardware

Industry Standards Software and Tools

Productive and Sustainable

Did you know?

All modern processors and systems use parallelism for performance.
Common Intel® architecture enables applications to run across the full spectrum of Intel® Xeon® family based servers so programmers don’t have to “start over”.

Use the same development tools you used for Intel® Xeon® processors with Intel® Parallel Studio XE 2015
Tick-Tock Development Cycles
Integrate. Innovate.

Intel® Core™ Microarchitecture
- Sandy Bridge Microarchitecture
- Haswell Microarchitecture
- Future Microarchitectures

Tick
- 45nm
- 32nm
- 22nm
- 14nm
- 10nm

Tock
- Nehalem Microarchitecture
- 3D Tri-Gate
- 2nd Gen Tri-Gate

Projection

SSE4.2/AESNI
AVX
AVX2**
AVX-512**

**Intel® Architecture Instruction Set Extensions Programming Reference, #319433-012A, FEBRUARY 2012
**Intel® Architecture Instruction Set Extensions Programming Reference, #319433-015, JULY 2013

Potential future options, subject to change without notice.

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# Intel® Xeon® Processor E5-2600 v2

„Ivy Bridge EP“

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D Tri-Gate Process</td>
<td>22 nm</td>
</tr>
<tr>
<td>ISA</td>
<td>AVX, SIMD-256</td>
</tr>
<tr>
<td>Up to 12 Cores</td>
<td>Up to 3.5 GHz Base Frequency</td>
</tr>
<tr>
<td>Up to 1866 MHz DDR3 Memory</td>
<td>Up to 768 GB Memory Capacity†</td>
</tr>
<tr>
<td>Integrated 40 Lanes PCIe* 3</td>
<td>Up to 8.0 GT/s QPI</td>
</tr>
<tr>
<td>Up to 12 Cores 24 Threads</td>
<td>Up to 30 MB L3-Cache</td>
</tr>
<tr>
<td>Up to 259 GFLOPS (DP-F.P. peak)</td>
<td>Up to 8.0 GT/s QPI</td>
</tr>
</tbody>
</table>

† depending DIMM capacity availability

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# Intel® Xeon® Processor E5-2600 v3

"Haswell EP"

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D Tri-Gate Process</td>
<td>22 nm</td>
</tr>
<tr>
<td>Up to Cores</td>
<td>18</td>
</tr>
<tr>
<td>36 Threads</td>
<td></td>
</tr>
<tr>
<td>Up to Base Frequency</td>
<td>3.5 GHz</td>
</tr>
<tr>
<td>ISA</td>
<td>AVX2 SIMD-256</td>
</tr>
<tr>
<td>ISA</td>
<td>TSX Transactional Synch</td>
</tr>
<tr>
<td>Up to Memory Capacity</td>
<td>768 GB</td>
</tr>
<tr>
<td>Integrated PCIe*3 Lanes (40GB/s)</td>
<td>40</td>
</tr>
<tr>
<td>Up to QPI (2x)</td>
<td>9.6 GT/s</td>
</tr>
<tr>
<td>Standard Processor TDP (with integrated VR)</td>
<td>60-145 W</td>
</tr>
<tr>
<td>Up to Peak Memory Bandwidth</td>
<td>68.2 GB/s</td>
</tr>
<tr>
<td>Up to Integrated</td>
<td>40 PCIe*3 Lanes (40GB/s)</td>
</tr>
<tr>
<td>Up to</td>
<td>*Other names and brands may be claimed as the property of others.</td>
</tr>
</tbody>
</table>

Potential future options, subject to change without notice. Codenames.

All timeframes, features, products and dates are preliminary forecasts and subject to change without further notification.

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Announcing

Intel® Omni Scale—The Next-Generation Fabric

- Designed for Maximum Scalability
- Rich Set of Programming Models
- Flexible Configurations
- End-to-End Solution

INTEGRATION

Intel® Omni Scale Fabric
Starting with Knights Landing

Intel® Omni Scale Fabric
Future 14nm generation

Coming in ‘15

PCIe Adapters ✓
Edge Switches ✓
Director Systems ✓
Intel Silicon Photonics ✓
Open Software Tools*

Intel® True Scale Fabric Upgrade Program Helps Your Transition

*OpenFabrics Alliance
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Unveiling Details of Knights Landing
(Next Generation Intel® Xeon Phi™ Products)

Compute: Energy-efficient IA cores
- Microarchitecture enhanced for HPC
- 3X Single Thread Performance vs Knights Corner
- Intel Xeon Processor Binary Compatible

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors
- up to 16GB at launch
- 1/3X the Space
- 5X Bandwidth vs DDR4
- 5X Power Efficiency

On-Package Memory:
- Integrated Fabric
- Intel® Silvermont Arch.
- Enhanced for HPC

Jointly Developed with Micron Technology

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice. Over 3 Teraflops of peak theoretical double-precision performance is preliminary and based on current expectations of cores, clock frequency and floating point operations per cycle. FLOPS = cores x clock frequency x floating-point operations per second per cycle. Modified version of Intel® Silvermont microarchitecture currently found in Intel® Atom™ processors. Modifications include AVX512 and 4 threads/core support. Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly codenamed Knights Corner). Binary Compatible with Intel Xeon processors using Haswell Instruction Set (except TSX). Projected results based on internal Intel analysis of Knights Landing memory vs Knights Corner (GDDR5). Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory only with all channels populated.

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Knights Landing

NERSC, CRAY, INTEL TO COLLABORATE ON NEXT-GENERATION SUPERCOMPUTER

APRIL 29, 2014 | Tags: NERSC

Contact: Jim Bashor, bashor@b1244p.nsl.sld.nra.gov, 510-485-5246

The U.S. Department of Energy’s (DOE) National Energy Research Scientific Computing (NERSC) Center and Cray Inc. announced today that they have signed a contract for a next-generation supercomputer to enable scientific discovery in the DOE’s Office of Science (DOE OSE).

Lawrence Berkeley National Laboratory (Berkeley Lab), which operates NERSC, collaborated with Los Alamos National Laboratory and Sandia National Laboratories to develop the technical requirements for the system.

The new, next-generation Cray XC supercomputer will use Intel’s next-generation Intel Xeon Phi™ accelerators — code names “Knights Landing” — a high-performance manycore processor with on-package high-bandwidth memory at Berkeley Lab’s new NERSC supercomputer. It is scheduled for delivery April 2015. The supercomputer will enable petascale scientific computing capability of NERSC’s system, a Cray XC supercomputer.

NERSC serves as the DOE’s primary high-performance computing (HPC) supporting more than 2,800 scientific projects in over 100 projects. The HPC supporting more than 2,800 scientific projects in over 100 projects. This 10-fold increase represents the DOE’s ongoing investment to advance the science and technology of high-end computing to address challenges such as developing new energy sources, improving energy efficiency, understanding climate change, advancing materials science, and more.

The new Cray supercomputer will be used to ensure the safety, security and effectiveness of the United States’ nuclear stockpile.

http://nnsa.energy.gov/mediaroom/pressreleases/04.01.10

Modernizing Community Codes...Together

Intel® Parallel Computing Centers

Plus...User Groups Forming

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