ChE 5480 Summer 2005 HPC Homework #1

Due in class Tue June 28 2005

Please feel free to discuss these questions with your classmates.

1. How many bytes worth of registers does a Pentium4 CPU have?

2. Name a difference between L1 cache and L2 cache.

3. What is a cache line?

4. Why do most contemporary computers have cache?

5. What is a cache hit?

6. What is a cache miss?

7. For each of these cache associativity schemes, a byte of RAM can go into how many different locations in cache?
   (a) direct mapped

   (b) fully associative

   (c) 2-way set associative

   (d) 8-way set associative

8. What is a cache conflict?

9. For each of these cache associativity schemes, what happens in the event of a cache conflict?
   (a) direct mapped

   (b) fully associative

   (c) N-way set associative (for some given N)

10. For each of these cache associativity schemes, are they popular? Why or why not?
    (a) direct mapped

    (b) fully associative

    (c) *N*-way set associative (for any given *N*)

11. Name two cache replacement strategies.
    (a)

    (b)

12. If a variable is in cache, is it also in RAM? Explain.

13. What does it mean for a cache line to be *dirty*?

14. What is the difference between *write-through* and *write-back*?

15. What is temporal data locality?

16. What is spatial data locality?

17. Typically, what will performance be if a code has little or no locality, compared to a code with a lot of locality?

18. What is *tiling*?

19. Why does tiling sometimes improve performance?

20. Under what circumstances would tiling not improve performance?

21. Why is hard disk slower than RAM?

22. Why should your hard disk I/O use binary representations rather than human-readable text?

23. Name an advantage of using a portable I/O library such as HDF or NetCDF, compared to outputting either native binary or text.

24. What is *virtual memory*?

25. A *page* in virtual memory is analogous to what in cache?